

Serial No. 09/741857

Art Unit: 2152

In the claims:

- 1 1. (currently amended) A method for processing a plurality of independent instruction threads
2 comprising: retrieving a first instruction from a first thread of instructions; retrieving a second
3 instruction from a second thread of instructions; executing the first instruction in a first stage of a
4 processing pipeline; and forwarding the first instruction to a next stage of the processing while
5 forwarding the second instruction to the first stage of the processing pipeline such that the first
6 instruction and the second instruction can be executed simultaneously in the processing pipeline,
7 and wherein the independence of the instructions threads eliminates pipeline processing delays.
- 1 2. (currently amended) The method for processing ~~a plurality~~ the plurality of independent
2 instruction threads according to claim 1, further comprising: transferring data from an input
3 buffer to a packet task manager; dispatching the data from the packet task manager to an analysis
4 machine; classifying the data in the analysis machine; and modifying and forwarding the data in a
5 packet manipulator.
- 1 3. (currently amended) The method for processing ~~a plurality~~ the plurality of independent
2 instruction threads according to claim 1, further comprising transferring the data after modifying
3 and forwarding to an output buffer.
- 1 4. (currently amended) The method for processing ~~a plurality~~ the plurality of independent
2 instruction threads according to claim 1, further comprising processing data at a rate of at least 10
3 Gbs.
- 1 5. (currently amended) An apparatus for processing a plurality of independent instruction threads,
2 said apparatus comprising: a processing pipeline including a plurality of stages coupled to
3 receive and process the plurality of independent instruction threads such that, during a processing
4 period, each of the plurality of stages of the processing pipeline is operating on a different one of
5 the instruction threads from the plurality of instruction threads, and wherein the independence of
6 the instructions threads eliminates pipeline processing delays.

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1 6. (original) The apparatus according to claim 5, further comprising; an analysis machine having
2 multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits
3 of a bit field; a packet task manager operationally connected to said analysis machine; and, a
4 packet manipulator operationally connected to said analysis machine.

1 7. (original) The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

1 8. (original) The apparatus according to claim 6, wherein said analysis machine has 32 threads.

1 9. (original) The apparatus according to claim 6, further comprising: a packet task manager
2 operationally connected to said analysis machine; a packet manipulator operationally connected
3 to said analysis machine; and a global access bus including a master request bus and a slave
4 request bus separated from each other and pipelined.

1 10. (original) The apparatus according to claim 6, further comprising: an external memory engine
2 operationally connected to said analysis machine; and a hash engine operationally connected to
3 said analysis machine.

1 11. (currently amended) The apparatus according to claim 9, further comprising: packet input
2 global access bus software-program code, stored in a computer readable memory and operable
3 when executed to control a used-for flow of data packet information from a flexible input data
4 buffer to ~~an~~ the analysis machine.

1 12. (currently amended) The apparatus according to claim 9, further comprising: packet data
2 global access bus software-program code, stored in a computer readable memory and operable
3 when executed to control a used-for flow of packet data between a flexible data input bus and a
4 the packet manipulator.

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1 13. (currently amended) The apparatus according to claim 9, further comprising: statistics data
2 global access bus software code used for connection of ~~an~~the analysis machine to ~~a~~the packet
3 manipulator.

1 14. (currently amended) The apparatus according to claim 9, further comprising: private data
2 global access bus software code used for connection of ~~an~~the analysis machine to an internal
3 memory engine submodule.

1 15. (currently amended) The apparatus according to claim 9, further comprising: lookup global
2 access bus software code used for connection of ~~an~~the analysis machine to an internal memory
3 engine submodule.

1 16. (original) The apparatus according to claim 9, further comprising: results global access bus
2 software code used for providing flexible access to an external memory.

1 17. (currently amended) The apparatus according to claim 5, wherein associated with each
2 instruction thread is a thread identifier (TID) identifying a subset registers allocated to the
3 corresponding independent instruction thread, the subset of registers selected from among a set
4 of registers, and wherein the subsets associated with each one of the plurality of independent
5 instruction threads are unique. ~~9, further comprising: results global access bus software code~~
6 ~~used for providing flexible access to an external memory.~~

1 18. (original) The apparatus according to claim 9, further comprising: a bi-directional access port
2 operationally connected to said analysis machine; an input buffer operationally connected to said
3 analysis machine; and an output buffer operationally connected to said analysis machine.